

# Design and Performance Evaluation of a Redundant Binary Full Adder for Uniform Timing Delay

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**Abstract**—Concurrency and timing guarantee are critical for robust performance of cyber-physical systems (CPS). Traditional binary adders are unable to provide such guarantee, as the timing delay is dependant on bit width and data. We present a design of a redundant binary full adder towards resolving this challenge, and a performance evaluation by implementing it with 0.6  $\mu\text{m}$  CMOS technology. The design composes of three modules: binary-to-sign conversion, plus-plus-minus (PPM) adder and sign-to-binary conversion. The complete adder circuit was functionally verified using Virtuoso simulation, and the timing delays were compared with the conventional full adder circuits. Through Logical Effort optimization, 5 ns of the timing delay for PPM adder was achieved, which was constant for any bit width and independent of data. The design achieves reduced timing delay compared to common full adder circuits for 32-bit or higher number of bits. The design might be an attractive solution to provide uniform timing delay towards the CPS challenge.

**Index Terms**—Plus-Plus-Minus (PPM), carry free addition, CPS, Logical Effort, redundant binary full adder, timing delay.

## I. INTRODUCTION

Cyber-physical systems (CPS) are tight integration of the computation domains with the real-time physical processes [1-3]. Many engineered systems today consist of a large number of heterogeneous subsystems whose interactions are both crucial for the system to meet its design objective and potential sources of failure. Examples of such cyber-physical systems include information systems, transportation systems, bio-inspired systems, software-hardware systems, prognostics, health management and care systems, sensor networks, renewable energy systems, and so on.

Embedded systems are information processing systems embedded into enclosing products [2]. These systems have always been held to a higher reliability and predictability standard than general-purpose computing. Embedded systems allow ubiquitous implementation of CPS in real-world setting. In the transition to CPS, the expectation of reliability will only increase. In fact, without improved reliability and predictability, CPS will not be deployed into such applications as traffic control, automotive safety, and health care.

Arithmetic operations are critical for computer computations, specifically for embedded systems [4]. To meet the CPS requirements, the timings must be guaranteed and the operation must be concurrent. In this work, we investigated one of the arithmetic operations: the full adder. In ripple carry adder (RCA), the addition time increases linearly with the increase in number of bit width due to rippling of carry from LSB to MSB [5]. In carry lock ahead (CLA) adder, the addition time gradually increases due to increased logic for carry calculation and hence circuit complexity changes with increased bit width [6].

An alternative approach for addition with constant time delay is to apply redundant binary representation (RBR) [7,8]. RBR is a numeral system that uses more bits than needed to represent a single binary digit so that most numbers have several representations. RBR differentiates from the usual binary numeral systems including two's complement that uses a single bit for each digit. Carry-free addition is an attractive property of redundant sign-digit numbers, as subset of RBR. Redundant binary full adder (RBFA) uses redundant signed-digit numbers to allow carry free addition. To implement this adder, the redundant binary sign-digit (RBSD) operation is handled through the Plus-Plus-Minus (PPM) adder and consequently, there is no need for an explicit mechanism for that [9]. In this work, we designed a RBFA for carry free addition to achieve constant time delay for any bit width.

## II. SYSTEM MODEL

We have subdivided the complete adder design in three modules as shown in Fig. 1. One of the inputs of the PPM adder directly passes to the PPM adder and the other passes through binary-to-sign-digit converter. To get the final sum in binary as inputs, a sign-digit-to-binary converter is designed.

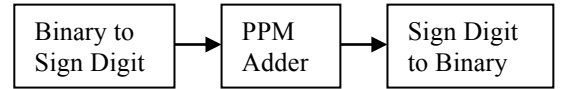


Fig. 1 Block diagram of three modules of the RBFA design

### A. Radix Number

A radix-2 RBSD number system is based on a digit set  $S \{1, 0, -1\}$ , where each digit can assume any of the three values from the set  $S$  instead of just the two values, 0 and 1, assign standard binary number system as shown in Table 1 [10]. Consequently, redundancy is introduced in the number system. Such representation is very advantageous while designing high-speed systems, since it allows carry-free addition.

TABLE 1  
Radix -2 Sign digit number representation

Sign Binary (SB)	Sign Digit (SD)	
	$X^+$	$X^-$
0	0	0
1	1	0
-1	0	1
0	1	1

The decimal value ( $D$ ) of RBSD number can be calculated by the following expression:

$$D = \sum_{i=0}^{n-1} x_i 2^i \quad (1)$$

where  $x$  is the bit values,  $i$  is the bit position, and  $n$  is the bit width. For example, the decimal number  $4_{10}$  can be represented in binary as  $0100_2$ . The same number in RBSD may be represented by more than one representations, i.e.  $(1 \bar{1} 0 0)$  or  $(1 \bar{1} \bar{1} 0 0)$ . Hence in this number system, a number can be represented by more than one way, called redundant representation. This redundant number representation, as shown in the example below in Table 2, allows the design for carry free addition.

TABLE 2  
Example of binary to RBSD representation

Binary Number	SD Number	$X^+$	$X^-$	$X^+$	$X^-$	$X^+$	$X^-$	$X^+$	$X^-$
0011	010-1	0	0	1	0	0	0	0	1
0111	100-1	1	0	0	0	0	0	0	1

### B. PPM adder

PPM adder performs the operation:  $x^+ + y - x^- = 2t^+ - u^-$ , which is an addition of a redundant number  $x$  (where  $x = x^+ - x^-$ ) to an unsigned binary number  $y$ , resulting in another redundant number expressed by an interim sum  $u^-$  and a transfer digit  $t^+$ . The input bits are defined as  $x^+, y, x^- \in \{0,1\}$  and the output bits are  $t^+, u^- \in \{0,1\}$ . PPM adder's truth table and block diagram are shown in Table 3 and Fig. 2, respectively.

TABLE 3  
PPM adder truth table

$X^+$	$Y$	$X^-$	$U^-$	$t^+$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

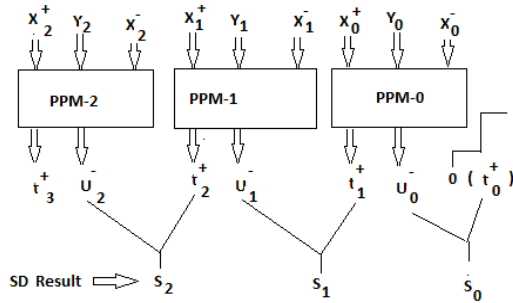


Fig. 2 PPM adder block

### C. SIGN DIGIT TO BINARY CONVERSION

The equation to get the final output ( $S$ ) in binary form is:

$$S = \sum_{i=0}^{n-1} t_i^+ * 2^i - \sum_{i=0}^{n-1} u_i^- * 2^i \quad (2)$$

The intent to convert RBSD to binary has stemmed from the conversion Table. 4. In Table 4,  $t^+$  and  $U^-$  are the 2

digits of the RBSD number,  $S$  is the corresponding binary output and  $C_{out}$  is the carry out which is fed to the next module. All carry propagation arising in addition can be avoided with the RBSD system, which is the primary reason for using it. Note that since a negative integer can be represented without any special sign-digit, it is possible to represent any integer and its negation with an equally number of digits.

TABLE 4  
Sign digit to Binary conversion

$t^+$	$U^-$	$C_{in}$	$S$	$C_{out}$
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1

## III. DESIGN

### A. Mathematical expression

Logical expressions for binary-to-sign-digit module can be based on design since redundancy is introduced in the system. We have represented logical expressions of binary-to-sign-digit converter, PPM adder and sign-digit-to-binary converter in (3), (4) and (5) respectively for 4 bits design though up to 16 bits has been designed for performance evaluation.

$$\left. \begin{aligned} x_0^- &= CD(\bar{A} + \bar{B}) \\ x_0^+ &= D(\bar{C} + AB) \\ x_1^- &= \bar{A}CB\bar{D} \\ x_1^+ &= C(AB + A\bar{D} + \bar{B}\bar{D}) \\ x_2^+ &= B(A + \bar{C}) + CD(A + \bar{B}) \\ x_3^+ &= C + AC + BC \end{aligned} \right\} \quad (3)$$

$$\left. \begin{aligned} \bar{z} &= x^+x^- + x^+x^- \\ U^- &= \bar{y}z + y\bar{z} \\ t &= x^+z + y\bar{z} \end{aligned} \right\} \quad (4)$$

$$\left. \begin{aligned} S &= t^+ \oplus U^- \oplus C_{in} \\ C_{out} &= C_{in}U^- + (C_{in} \oplus B)\bar{A} \end{aligned} \right\} \quad (5)$$

We have used the Virtuoso tool (Cadence Inc., CA, USA) for simulation using CMOS 0.6  $\mu m$  technology. The complete schematic is given in Fig. 3.

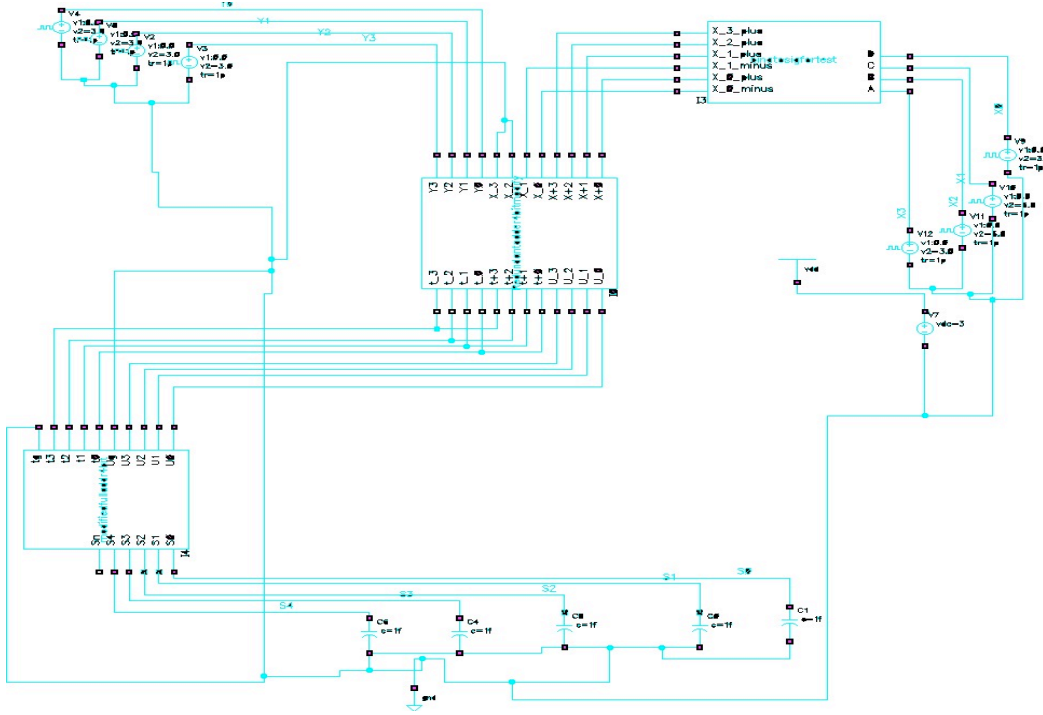


Fig. 3 Schematic diagram of RBFA circuit

### B. Optimization of PPM module

In our work, we have optimized the path delay of PPM adder as shown in Fig. 4 using Logical Effort technique by optimizing the size (width) of the transistors to reduce the delay. First, we find out the path which gets maximum time for various input combinations, called the critical path, as shown in Table 5 and Table 6 then optimize the logic transistors along this path based on the equations in text book [11]. In our design we have optimize the interim sum path.

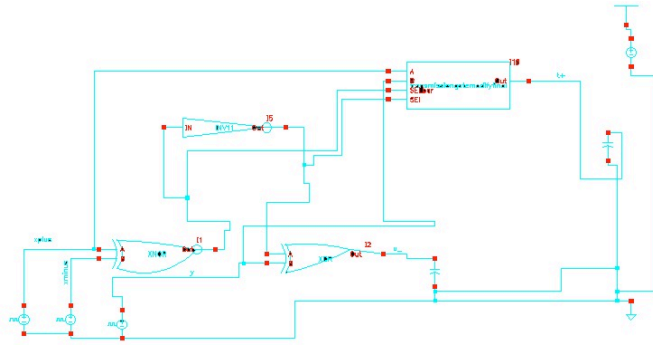


Fig. 4 Schematic diagram of a PPM adder unit for delay optimization

Before optimization, the critical path delay for PPM adder was 6.6 ns. After optimization, the delay reduced to 5 ns. This delay is constant for any number of input bit width.

TABLE 6  
PPM adder transfer bit delay calculation

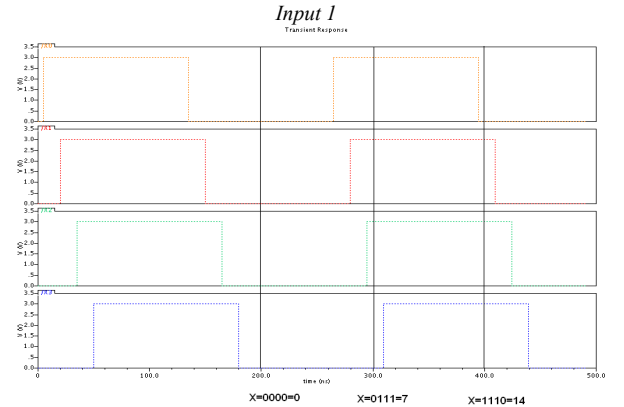
INPUT STATE FOR TRANSFER BIT	T+	
	TPL-H(NS)	TPH-L(NS)
$x^+=1, x^-=0>1, Y=1$	28.8-24=4.8	
$x^+=1>0, x^-=0, Y=1>0$		104.7-100=4.7
$x^+=1, x^-=0, Y=0>1$	204.6-200=4.6	
$x^+=0, x^-=1>0, Y=1$		279.9-275=4.9
$x^+=1, x^-=1>0, Y=0$		379.8-375=4.8

### IV. RESULTS

From the representative output graphs given in Fig. 5, the functionality of the complete adder circuit is verified. The results from some instances are given here:  
Input at 200ns: X=0000, Y=1110, the output is S=01110.  
Input at 300ns: X=0111, Y=1000, the output is S=01111.

TABLE 5  
PPM adder interim sum path delay calculation

INPUT STATE FOR INTERIM SUM	U-	
	TPL-H(NS)	TPH-L(NS)
$x^+=1, x^-=0>1, Y=1$		79.78-75= 4.78
$x^+=0, x^-=0>1, Y=0$	129.6-125=4.6	
$x^+=1, x^-=0, Y=0>1$		204.9-200=4.9
$x^+=1, x^-=0>1, Y=1$	230.4-223.8=6.6	
$x^+=0>1, x^-=1, Y=1$		254.7-250=4.7
$x^+=0, x^-=1>0, Y=1$	280.5-275.9=4.6	
$x^+=1, x^-=1>0, Y=0$		304.9-300=4.9
$x^+=1, x^-=1>0, Y=0$	379.5-375.1=4.4	
$x^+=0, x^-=0>1, Y=1$		429.8-425=4.8



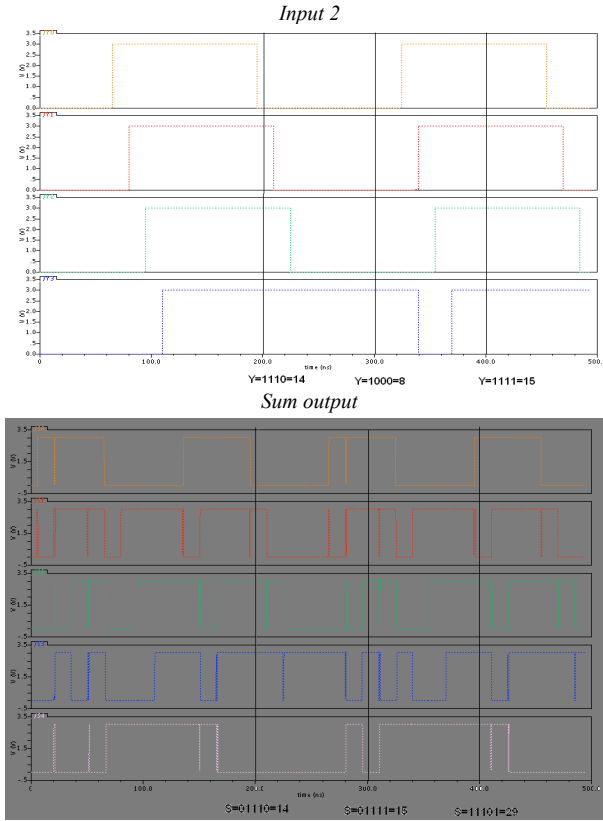


Fig. 5 Transient graphs of inputs and sum output of the RBFA circuit

## V. PERFORMANCE EVALUATION AND DISCUSSION

The total delay for RBFA will be sum of delay for one PPM adder, binary-to-sign-digit (BSD) conversion delay, and sign-digit-to-binary (SDB) conversion delay. SDB delay depends on carry, whereas other two delays do not depend on carry as shown in Fig. 6. Thus the total delay for larger bit widths is less affected in RBFA implementation, resulting more optimized timing performance for large number of bits through carry free addition.

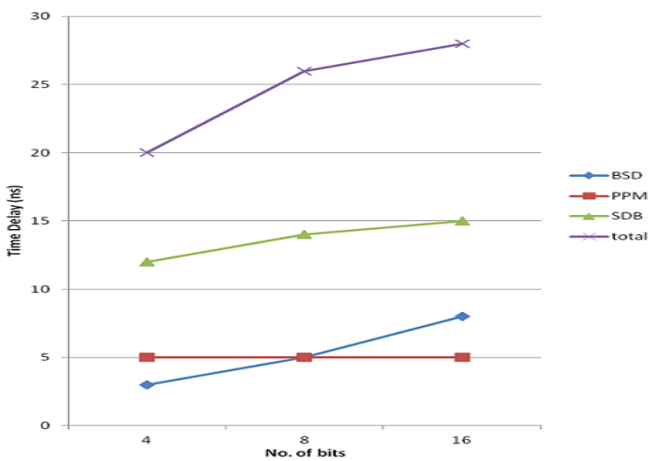


Fig. 6 Delay for the different module of the RBFA system

Timing delay performances of RCA, CLA and RBFA adders up to 16-bit width were simulated using Virtuoso simulator and their timing delay reports were observed, as shown in Fig. 7. Here the dotted lines indicate that those values are calculated based on the delay equations. It is observed that the delay produced in RBFA is higher when the number of bits is less than 16, but the delay remains almost

constant (40ns) for any number of bits. For larger widths of 64 bits, delay of RBFA is less compared to CLA and RCA. This is due to the fact that the delay for RCA will be the product of  $n$  (number of bits) and delay for one full adder. Similarly delay for CLA also increases with the number of bits. The CLA adders are faster up to 12-bit width and thereafter addition using RBFA is suitable for 64 or higher number of bits. RBFA also has an advantage of uniform timing delay for any number of bits, which is suitable for CPS systems.

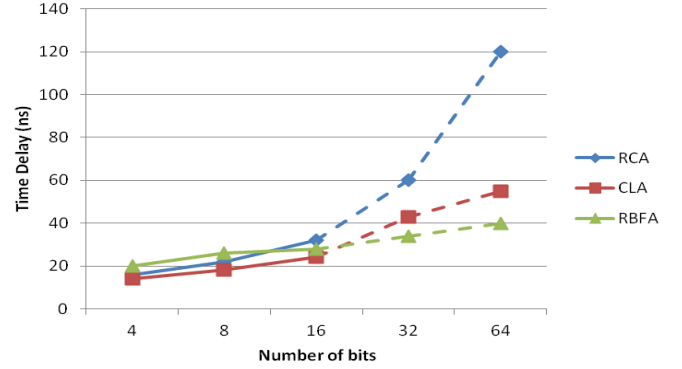


Fig. 7 Delay comparison among RCA, CLA, and RBFA system

## VI. CONCLUSIONS

Using RBFA design, it is possible to achieve uniform timing delays for addition operation, and hence guarantee the time requirement for the arithmetic operation. The design is also faster for larger bit width compared to conventional two's complement conversion, because for this conversion the total timing delay is proportional to  $\log(n)$ , where  $n$  is the bit width. Unlike RCA or CLA adder, the addition in a RBFA maintains a constant time irrespective of bit width, as each result bit is calculated independently, achieving concurrency and providing timing guarantee. The design can be used in computer arithmetic units and other computational hardware to address the timing challenge of CPS. Optimization based on number of transistor requirement and comparison with other adders based on timing delays, number of transistors and power dissipation is a future research direction.

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