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Power Optimization of NeuroMonitor EEG Device: Hardware/Software Co-Designed Interrupt Driven Clocking Approach*

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***Abstract*— Wireless and wearable EEG device for home based long-term non intrusive diagnosis for therapy applications like ASD, ADHD, Epilepsy and other neurological disorders is crucial. This work presents the NeuroMonitor (*rev.* 2.0) platform designed to record EEG signals from two (bipolar or referential montage) channels. The device is lightweight** $41.8g$ **(with** $900mAh$ **battery and 3 electrodes) and miniature,** $5.58cm \times 2.03cm \times 0.91cm$**. A power analysis and power optimization techniques have been studied using interrupt driven clocking approach for the Analog Front End, the ADC and the Digital Back End. About 5 fold power reduction; from the** $94mW$ **(av.) in** *rev.* 1.0 **to a** $17mW$ **in** *rev.* 2.0**, while maintaining the sampling rate has been achieved.**

I. INTRODUCTION

Human scalp electroencephalogram (EEG) can monitor the brain activities that relate to mental states, stimulations and activities. EEG signals are classified as delta (0.1-3.5 Hz), theta (4-7.5 Hz), alpha (8-13 Hz), beta (14-30 Hz) and gamma (>30 Hz) [1]. Neuroscientists have identified regions of the brain responsible for specific activities (lobes). Prefrontal lobe is highly associated with problem solving, mental flexibility, judgment, creativity [2] and deficiencies typical for ASD whereas temporal lobe is primarily responsible for auditory sensation, perception, language comprehension, long-term memory and sexual behavior [3].

Despite the fact that commercial wireless EEG systems exist [4][5], none of the currently available devices are practical to be used in the natural settings to record brain activities of, for instance, children with development delays in classroom settings or at home. The existing devices are large and uncomfortable to wear by children; they are either harness or helmet based and are visually identifiable; which might lead to deviation or shift of cognitive activities. With this prospective, we have developed an ambulatory EEG NeuroMonitor Platform [6].

This paper presents a revised (*rev* 2.0) design of a miniature two channel, wireless EEG data acquisition system that can record continous brain activities for long periods (> 3 days) . The developed EEG system can be concealed within a headband or a cap or other accesories, so that it can be worn comfortably in natural settings for long duratiosn. A novel power optimization approach is reported in this paper.

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II. EMBEDDED HARDWARE DESCRIPTION

The PCB was designed using Cadence Allegro SPB 15.5 (Cadence Design Systems, Inc., San Jose, CA, USA) and measures $5.58cm \times 2.03cm \times 0.91cm$, weights $41.8g$ and was fabricated at Advanced Circuits (Aurora, CO, USA). The hardware of the NeuroMonitor with 2 independent channels in either bipolar or referential montage, can be divided into four different blocks: Analog Front End (AFE), sampling, Digital Back End (DBE), and data storage/transmission (Fig. 1).

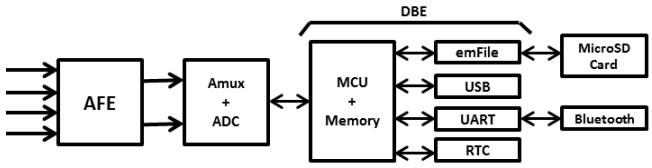

Fig. 1. Block diagram of the Neuromonitor hardware system where all the blocks, including most components from the AFE, are within the PSoC.

A. Analog Front End (AFE)

In Fig. 2 the schematic for the AFE is shown, comprised of by two channel differential Instrumentation Amplifier, ISL28270 (Intersil Americas, Milpitas, CA, USA) that amplifies the raw EEG signals captured by the GS-26 pregelled EEG/EMG electrodes (Bio-Medical Instruments Inc., Warren, MI, USA). The signal is then notch filtered ($f_n = 60Hz$) with a modified Twin T Notch Filter [7] implemented on the two channel MCP6002 (Microchip Technologies Inc., Chandler, AZ, USA) Operational Amplifier (OpAmp).

Next, a 2^{nd} order active Low Pass Filter (LPF) Chebyshev-I filter is cascaded by a 2^{nd} order passive LPF with overall $f_c = 125Hz$. The LPF uses the internal OpAmps from the Programmable System On a Chip (PSoC, Cypress Semiconductor Corp., San Jose, CA, USA). A High Pass Filter (HPF) with $f_c = 0.5Hz$ is then followed by a DC bias circuit to offset the signal for the Analog to Digital Converter (ADC). The last AFE stage is a non-inverting amplifier that uses the OpAmps from the PSoC to ensure the final total gain of $72dB$.

The 3 different DC bias used in the AFE are sourced from the 8bit DACs with $V_{ref} = 1.024V$ from the PSoC that gives us the flexibility to adapt the system to any subject regardless of body biopotential. The magnitude and phase Bode plots of the AFE is shown in Fig. 3.

The input/outputs of the OpAmps in the PSoC have been placed in the preferred input/output pins that minimize the

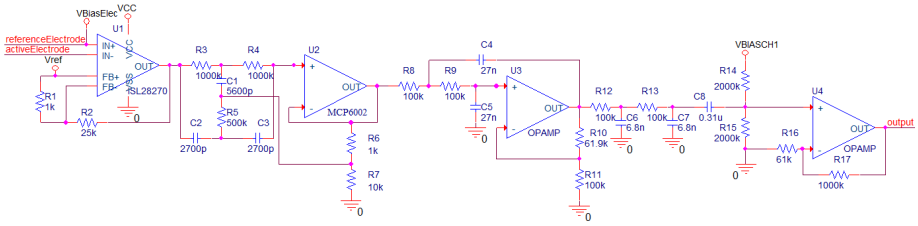

Fig. 2. Schematic diagram of the Analog Front End (AFE) for each channel of the NeuroMonitor (*rev* 2.0).

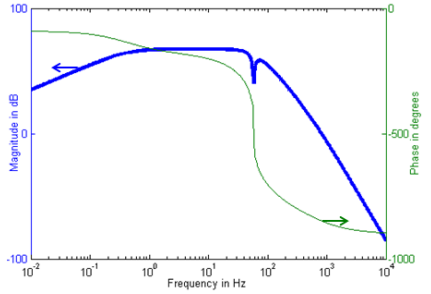

Fig. 3. Magnitude (Think Blue) and Phase (Thin Green) Bode plot for the AFE with component values inserted in the simulation. $f_{lc} = 0.48Hz$, $f_{hc} = 126Hz$ and $f_{notch} = 58.8Hz$

capacitance and resistance as well as freeing analog routing resources. Since we are using almost all the analog resources of the PSoC 3, the analog routing is maxed out, which means that signals that could have been routed internally, like the last OpAmp to the ADC, had to be routed externally in the PCB.

B. Sampling circuitry

The digitization of the analog signal is done by a single ended 16b Delta-Sigma ADC at $256sps$ running at $10MHz$ with $V_{ref} = 3.3V$. The two channels are sampled after being multiplexed by an internal Analog Multiplexer (AMux). The ADC is configured in the Single Sample mode and performs one sample conversion when requested. The ADC stays in standby waiting for the start sampling signal. When this happens, the ADC performs the conversions.

C. Digital Back End

The core of system is the CY8C3866-030LTI, from the PSoC 3 family, which is an embedded microcontroller with an array of configurable analog and digital blocks. The Micro-Controller Unit (MCU) is an optimized single cycle 8051 core with access to 64KB of flash, 8KB of SRAM and 2KB of EEPROM. As for the other in-built blocks, this work uses the 4 OpAmps available as well as 4 DACs and the ADC, as already described. Other modules used are the UART controller that is used to communicate to a Bluetooth module, the emFile block which manages the read/write operations to a micro SD-Card in FAT32, a Real Time Clock (RTC) and a USB 2.0 device controller.

D. Storage and transmission

External components to the PSoC, the NeuroMonitor system contains a microSD card, a RN-42 Class-2 Bluetooth device (Roving Networks, Los Gatos, CA, USA) configured with SPP profile and an RGB LED for user feedback. The current system is powered by a $900mAh$ Lithium Polymer battery (Tenergy Corp., Fremont, CA, USA), and the charging is managed by MCP73831 (Microchip Technology) charger using the microUSB connector available in the board.

III. Embedded Software and Functionality

A graphical user interface (GUI) was created using Visual Basic.Net (Microsoft Corp., Redmond, WA, USA) and it provides the ability to synchronize and configure the board. Two operating modes can be chosen: 1) Online - where the recorded EEG signals will be sent wirelessly to a PC in real-time, or 2) Offline - where EEG signals will be saved on the onboard microSD card in a file. Other items that can be configured are the record details, like Subject ID, Experiment start time, Experiment ID, EEG Device ID, etc. This parametric information is saved as header in the file.

A. Firmware

After start-up, the PSoC waits until the time is synchronized. Then, PSoC waits for the mode to be set. If user has selected Online mode, the Bluetooth module remains on the sniff mode, but if Offline mode is selected, Bluetooth is turned off once the synchronization is over.

As explained in the previous subsection the sampling rate is $256sps$ which is accomplished by interrupting the MCU every $3.9ms$ and requesting a sample from the two channels, one after the other by switching the AMux. In the Interrupt Service Routine (ISR), two buffers each $256B$ is used to save the sampled raw EEG data from the ADC. Once one array is full, the other starts saving the data and the data of the full one is saved in the microSD card or transmitted to the remote device wirelessly.

B. Functional Results

After testing the board with known sinusoidal input signals to verify performance, raw EEG data was collected with the two active electrodes on the prefrontal cortex at FP1 and FP2 and the reference location was the left mastoid. The protocol for data collection asked the subject to relax for 1 minute and the subject was advised to minimize the blinking and frowning. The EEG results for FP2, which corresponds to channel 2 of the AFE, is shown in Fig.4 after applying a digital notch ($f_n = 60Hz$) filter in MATLAB (Mathworks Inc., Natick, MA, USA).

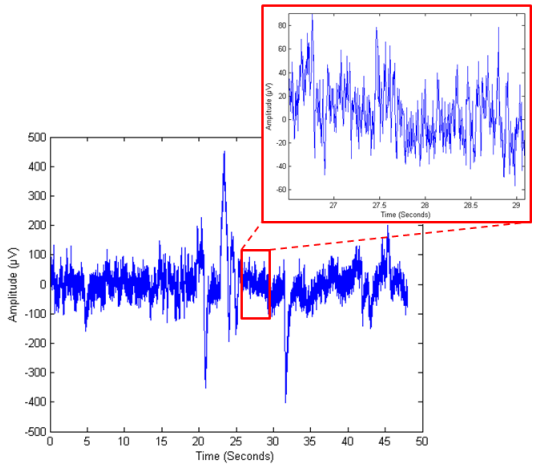

Fig. 4. Spline and notch filtered EEG from prefrontal lobe location FP2

IV. POWER ANALYSIS

In the previous report of the Neuromonitor device, power consumption was not the main focus since a functional system was prioritized [6]. Here we study the power optimization approach in greater details.

We have used a hardware/software co-design approach for power optimization. The hardware measures were based in careful component selection to reduce the number of components and their power consumption. From the firmware level; power optimization measures like the Sniff mode in the RN-42 (which puts the device to sleep every $100ms$, then wakes up for $5ms$) is used. In this setup, when there is any data to transfer, it sends the data to the remote device (PC), then it returns to sleep, and the process repeats. Other techniques implemented are the buffering of the sampled data to minimize the time the microSD Card (up to $100mA$ when read/write) or the BT are ON (up to $36mA$ when transmitting).

The power consumption of our system can be divided in $P_{Total} = P_{AFE} + P_{ISR} + P_{DBE} + P_{Storage/Trans.}$, where P_{AFE} is the power consumption of the AFE, P_{ISR} for the ISR (ADC + AMux + ISR code), P_{DBE} of the PSoC (excluding ISR) and $P_{Storage/Trans}$ is the power consumption to store or transmit data. In this study, we focus on power reduction of the first three stages P_{AFE}, $P_{Sampling}$ and P_{ISR}.

A PCB with only one channel of the AFE and the PSoC was soldered. From the original firmware only the ISR and the configuration lines for the AFE were kept, everything that was not AFE or sampling related was eliminated for a correct measurement and fair comparison.

The current measurements were taken using a $\mu Current$ device (eevBlog, Sydney, NSW, AU). It was set at the $1mV/1mA$ range and the output voltage was connected to a TDS1001B oscilloscope (Tektronix, Beaverton, OR, USA). The power supply used was a E3631A (Agilent Technologies Inc., Santa Clara, CA, USA) with fix $3.3V$ from the $6V$ rail.

For the measurements where time was measured, one of the RGB LED (not populated) pins was used as trigger for the oscilloscope. Standard to all measurements, the MCU ran a $while(1)$ with two $for\ loops$ that incremented a variable and another RGB LED pin (not populated), was set and cleared in the loop. The code is written in PSoC Creator using level 5 optimizations in the compiler.

A. Startup power consumption

By default when the PSoC is powered up is set to Fast Internal Main Oscillator (FIMO) mode, which means that IMO frequency is $48MHz$ [8] . Instead of starting with the IMO at $48MHz$ the PSoC is powered up at nominal frequency ($3MHz$). In Fig. 5, the transient current consumption of the board is shown. When averaging the current consumption over the startup time ($25.42ms$ for FIMO and $34.14ms$ for nominal IMO), the current consumption for FIMO was $4.82mA$ while for the nominal IMO was $3.36mA$. Despite affecting only in the startup, it might be important for systems that are not be able to provide such currents, like systems powered by energy harvesting techniques.

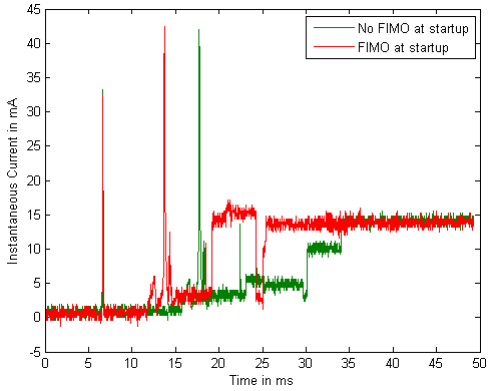

Fig. 5. Start-up transcient current for FIMO (red) and nominal IMO (green). The first spikes are due to decoupling capacitor charging.

B. AFE Power Consumption

The AFE is comprised of the ISL28270, the MCP6002, the passives, the 2 internal OpAmps from the PSoC, and 3 DACs from the PSoC as shown in Fig. 2. For each internal component of the PSoC, as well as for the Instrumentation Amplifier, the power was measured while the rest of the components were power gated. In Table I, a summary of power consumption as well as the wakeup time from sleep mode to functional mode is shown.

TABLE I
CURRENT CONSUMPTION OF AFE COMPONENTS AND WAKEUP TIMES

Component	Current Consumption	Wakeup time
Instrumentation Amplifier	$217\mu A$	-
OpAmp	$400\mu A$	$6.3\mu S$
Vref DAC	$300\mu A$	$62\mu S$
VBIASCH1 DAC	$270\mu A$	$17.7\mu S$
VBiasElec DAC	$310\mu A$	$16.7\mu S$

After analyzing each component, a functional analysis was done using a DG4062 (Rigol Technologies Inc., Beijing,

China) signal generator outputting a sine wave of $2mV_{pp}$ at $10Hz$ and then attenuated. The signal was measured at the last stage of the AFE using the oscilloscope. It was found (Fig. 6) that the transient time when power switches from 0 to $3.3V$) is too long ($> 3s$) for our system to be able to put the analog component to sleep.It takes at least $1.5s$ for the signal to overcome the transients and around $3s$ to reach steady-state which makes it not usable since we $< 3.9mS$.

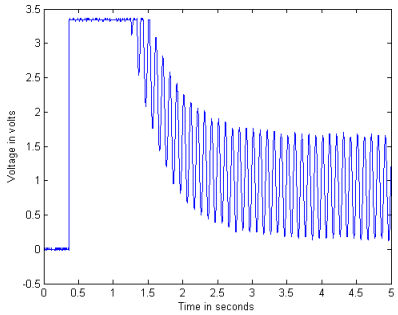

Fig. 6. Analog Front End transient time.

C. ISR Power Consumption

The ADC and the AMux can be put to sleep and woken when necessary without affecting functionality, since the ADC and Amux are triggered to acquire a sample.

When the ADC is in stand-by it consumes $2.5mA$ while the stand-by current of the AMux is $150\mu A$. When the MCU goes into the Interrupt Service Routine (ISR), both AMux and ADC are woken up using the API, the channels are sampled, takes $242\mu s$ to finish; and both components are put to sleep until next interrupt.

There might be still a few computations that will need to be done by the MCU, so the dynamic clock system was investigated. In this case, after some previous studies, it was determined that a $3MHz$ clock should suffice, however, the ADC requires at least $10MHz$. In the ISR before any sampling is done, the clock is increased dynamically from $3MHz$ to a higher frequency of at least $12MHz$.

TABLE II
AVERAGE CURRENT CONSUMPTION FOR DIFFERENT FREQUENCIES/MODES

Component	Average Current Consumption
Original [6]	$28.4mA$
NF(3MHz), SUF(62MHz)	$18.72mA$
NF(3MHz), SUF(48MHz)	$5.42mA$
NF(3MHz), SUF(24MHz)	$5.35mA$
NF(3MHz), SUF(12MHz,Flash Optimal)	$5.24mA$
NF(3MHz), SUF(12MHz)	$5.35mA$
NF(12MHz,ADC off),	$8.32mA$
NF(12MHz, ADC on)	$10.9mA$

Different frequencies speed-ups and configurations where tested to find the optimal frequency/mode that would reduce the average power consumption. In Table II the average current consumption for the different frequencies speed-ups/modes from Fig. 7 is shown.Only the IMO frequency was changed since the PLL consumes $300\mu A$ extra.

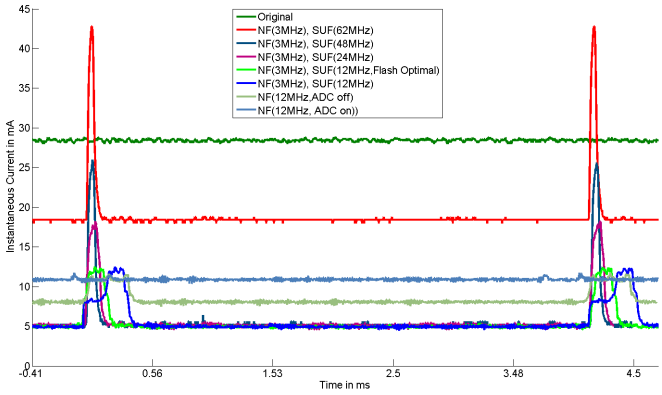

Fig. 7. Power comsuption with different frequency and mode values. NF = Nominal Frequency and SUF = Speed-Up Frequency.

V. CONCLUSIONS

This work presents the NeuroMonitor platform designed to record EEG signals from two (bipolar or referential montage) channels. The device is lightweight $41.8g$ (with $900mAh$ battery and 3 electrodes) and miniature ($5.58cm \times 2.03cm \times 0.91cm$). This work demonstrates interrupt based clocking reduces the current consumption drastically, from the $28.4mA$ average current to a $5.24mA$ when the new techniques are applied. It was found that for our application, using the minimum clock allowed ($12MHz$) minimized the power consumption to $17.29mW$.

The power consumption with either data storage or transmission can be estimated to be under the $33mW$, down from the $135mW$, leading to a 90hr of continuous operation with a $900mAh$ LiOn battery. Such power optimization is necessary for home based monitoring, so that the device only needs to be recharged overnight and twice a week.

ACKNOWLEDGMENT

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